ENGR xD52: Midterm

Due before class on 10/24 to comparch13@gmail.com with subject "[Midterm] – Your Name"

Honor Code Policy

This midterm is to be done entirely on your own with no assistance from or collaboration with other humans. However, you do have free access to my slides, your notes, the internet, textbooks, ModelSim, etc. Document exactly which resources you use, including specific URLs.

Summary

The goal of this exercise is to faithfully recreate (the electrical portion of) a real product that is currently available for sale as faithfully and as cheaply as possible. For this, we are using a safety light for a bicycle that features several modes of operation.

Specification Document

Write a brief but informative specification document that clearly captures the design intent of the digital electronics portion of the product. This should include:

- All operational modes of the product (blink patterns)
- How the product changes operational modes
- Measurements of relevant dimensions in appropriate units with actual numbers – e.g 10 Hz, rather than "quickly"

This should not include:

- Any information about the mechanical aspect of the product, other than that required to communicate about the electrical portion.
- Implementation details. Answer "What", not "How"

Done well, this should be roughly one page including figures and/or charts.

Block Diagram / Schematic

This is where you get to answer "How".

Design a digital circuit that implements the Specification Document. Limit yourself to the following components:

AND, NAND, OR, NOR, XOR, XNOR, NOT, Buffer, MUX, Decoder, LUT, Edge-triggered D-Flip Flop. If you require additional components, build them out of these components hierarchically.

The deliverable for this portion is a hierarchical schematic document that shows your design. Each new level of hierarchy should be on its own separate page. For reference, my design took less than 10 pages.

Hint: You may concatenate multiple signals together to drive the address pins of a LUT.

Cost Estimation

Estimate the cost of your design in terms of area of silicon consumed. For this, we will assume that cost linearly scales with the number of gate inputs for basic inverting gates. Non-inverting gates cost 1 extra for the implicit inverter.

Gate	Cost
Inverter	1
2 Input NAND gate	2
2 Input AND gate	2+1=3
N Input NOR gate	N
Edge Triggered D-Flip Flop	13
LED Drive Circuit	211
Oscillator	100
Button Input Circuit	???
W width D depth LUT	???

Extra Credit

Reduce the total cost of your circuit.

Free Components

I have started three of the components for you. Notice how each component is a small example of the type of thing you are producing on this exam (specification, schematic, cost).

LED Driver

Specification

The LED Driver Subcircuit provides power to the indicator LED.

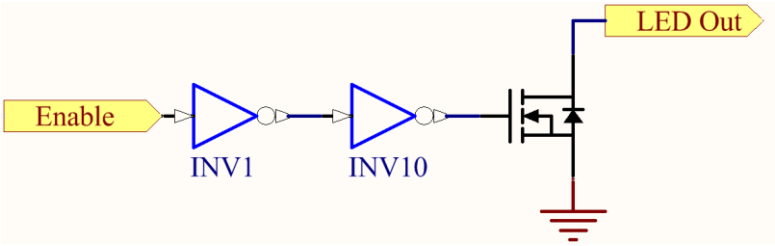
Inputs:

> Enable – Active High Input. When this input is high, the LED is provided power and will light.

Outputs:

> LED Out – Open Drain Output. Sinks current to ground when active. High Impedence when not active. Connect to the cathode of the LED. Connect anode of LED to positive power rail through limiting resistor to ensure no more than 20mA.

Schematic



Cost

The final output transistor is oversized in order to handle the LED current. It consumes the 200 Gate Input Equivalent space. The inverter that drives this transistor is 10 times larger than normal. The first inverter is normal sized, and is 1 Gate Input Equivalent. The total cost is therefore 211 GIE.

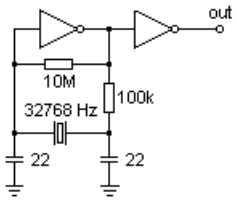
Oscillator

Specification

The oscillator sub-circuit provides a 32,768 Hz square wave whenever power is applied.

Parameter	Nominal	Min	Max	Notes
Frequency	32768 Hz	-200ppm	+200ppm	0 – 70 Celsius
Duty Cycle	50%	45%	55%	
Jitter			150ns	
Start up time	90 us	----	120us	
Maximum Load			10k GIE[1]	
Silicon Area Used	100 GIE			

Schematic



Cost

Several off-die components are not factored in to the space cost of this circuit – the crystal and the capacitors. The driving inverters and the associated resistors combine to consume 100 GIE.

[1] Gate Input Equivalent

Button Input

Specification

The Button Input Circuit filters the user button in two ways:

1) It ensures that changes are only presented to the rest of the circuit when the clock ticks.
2) It attempts to filter out the “switch bounce”, where the button wire will oscillate quickly when the switch is pushed.

Inputs:

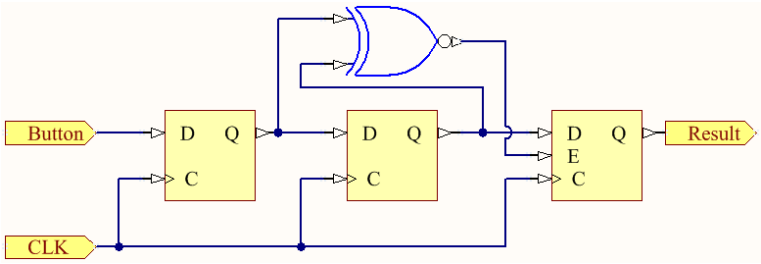
Clock: A 32768Hz clock signal. The output will be updated on the Positive edge of this clock.

Button: The unfiltered wire attached to the user button. High when the button is being pushed by the user. Low otherwise.

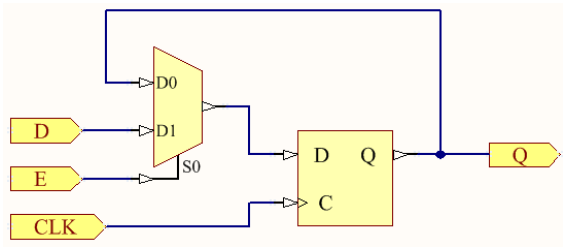
Outputs:

Result: Active High Output – High when the button is being pushed by the user, low otherwise.

Schematic



Subcircuit: D-Flip Flop with Enable



Cost

The two D Flip Flops without enable are known to use 13 Gate Inputs, as it is listed on the chart above. The third D Flip Flop has an enable, which is implemented with an added two input mux . The two input mux contains (*MESSAGE REDACTED, DO THIS PART YOURSELF*), for a total of M Gate Inputs. The XNOR gate contains (*SORRY, MORE WORK FOR YOU NOT ME*), for a total of X Gate Inputs. The total cost is therefore:

Gate Type	Size	Number Used	Total
Edge Triggered DFF	13	3	39
2 Input MUX	M	1	M
2 input XNOR	X	1	X
			39+M+X

Notes:

This exam builds on itself very linearly. If you are confused by an early portion, please speak with me as soon as possible so that the later portions can be salvaged.

The above option depends heavily on whether you have internalized the Toothpaste For Dinner – Creative Process comic I posted on the first day in the syllabus.