# Specification for timing module in RGB-to ARINC818 converter

## Inputs

* PCLK: Pixel clock
* HS: Horizontal synchronization signal
* VS: Vertical synchronization signal
* SCDT: Active high signal indicating that video is being converted
* DE: Active high signal indicating that active pixel data is being presented
* REFCLK: internal FPGA reference clock of known frequency

## Outputs

* Start\_frame: pulses high when a new frame is about to begin
* Valid: Active high signal indicating that valid (correct resolution and refresh rate) video is present
* Store: Active high signal which becomes high whenever valid video is coming in and the present pixel is in the active region.
* Flush: pulses high on the first frame of a valid video signal.

## Requirements

1. Start\_frame is active for at least one cycle of PCLK, only goes active after the last active pixel of the previous frame, and goes inactive before the start of the active region of the next frame.
2. Valid remains high as long as valid video is present.
3. Valid only goes high when the presented video has the correct resolution and the correct refresh rate.
4. Flush is active for at least one cycle of PCLK, and goes inactive before the first active pixel of the first valid frame.
5. Store is active only on active pixels and only when valid video is present.